

High-Level System-on-Chip Simulator

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Microelectronic market

Consumer's requirements

are to get next production:

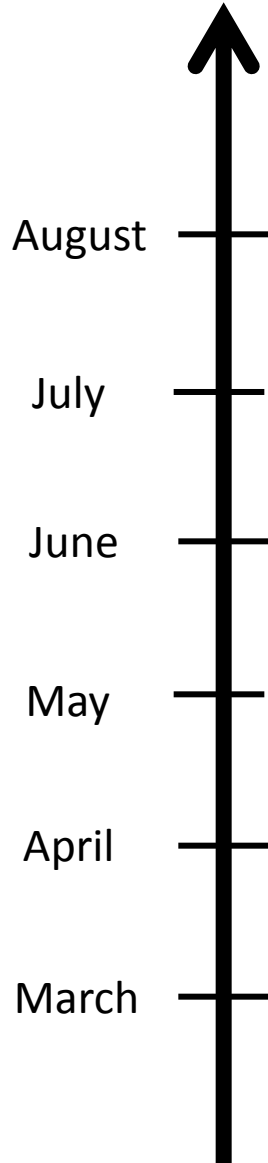
- high-speed
- reliable
- small-sized
- low-power

Manufacturer's task

Is to market their products as quickly as possible

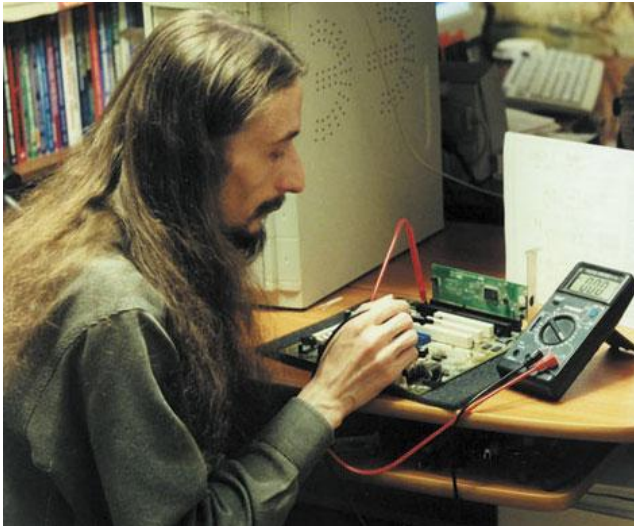


New product development



Software development

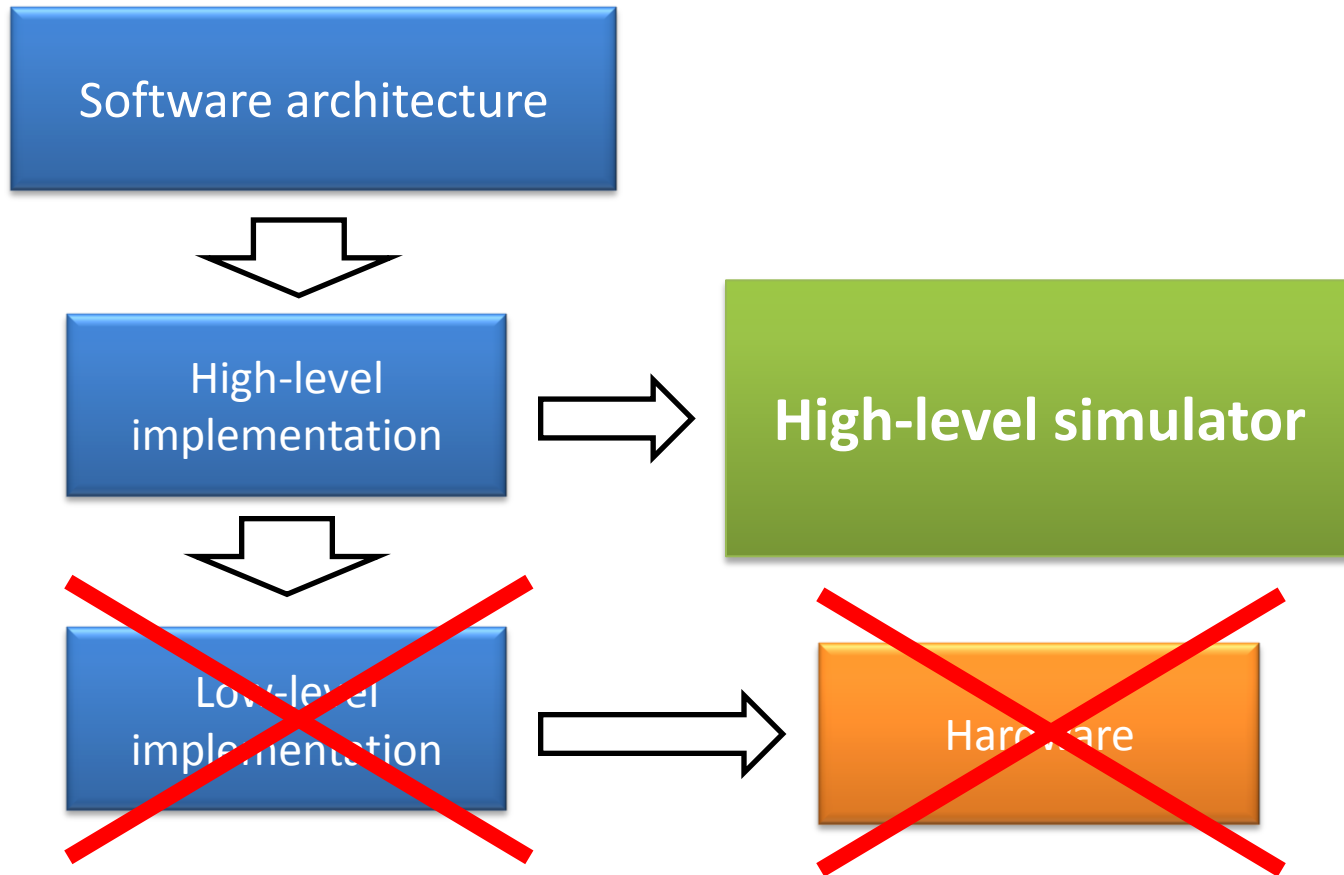
T1



Hardware development

T2

Software development



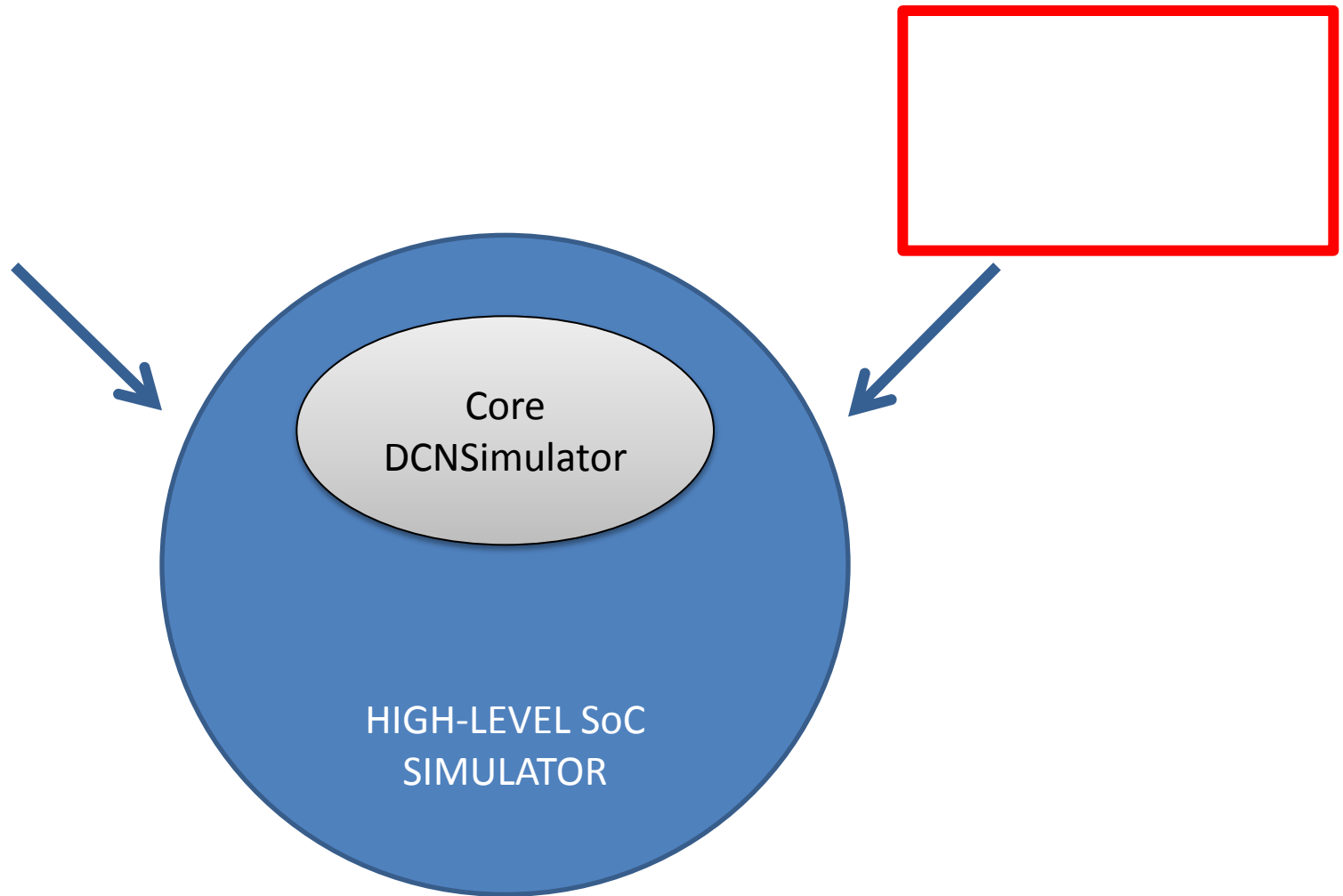
High-level simulator

1. allows rapidly and with minimal cost to
 - inspect
 - set
 - test real system program-logic model without its building
2. provides to a user an opportunity to invoke and debug software for this model on it.

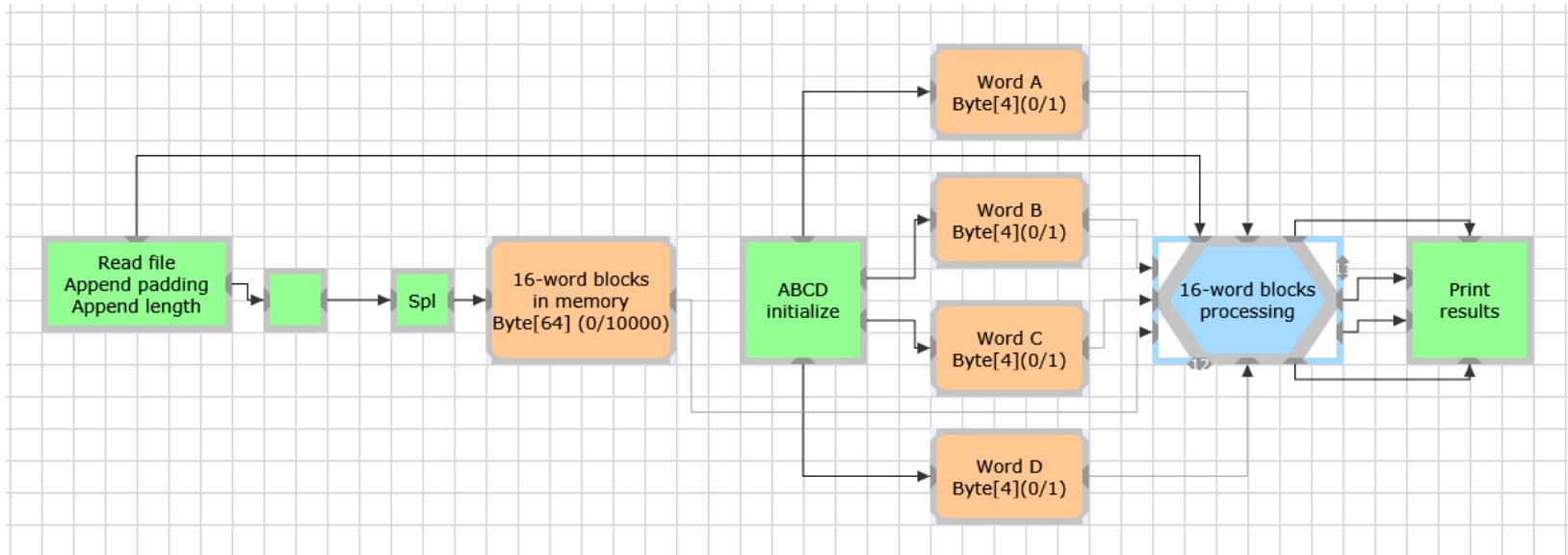
Requirements to simulator

- Provide an ability to model invoking high-level software presentation on the systems-on-chip model with an arbitrary configuration;
- Model the next hardware platform's characteristics:
 - delays of data packets sending and reception for each SoC device;
 - delays during data packets transmission through channels;
 - delays during program processes invoking on processing elements;
 - delays for accessing common memory etc.
- Collect statistical information about a simulation process;
- Show textual and graphical information after a simulation process is finished.

Simulator's structure

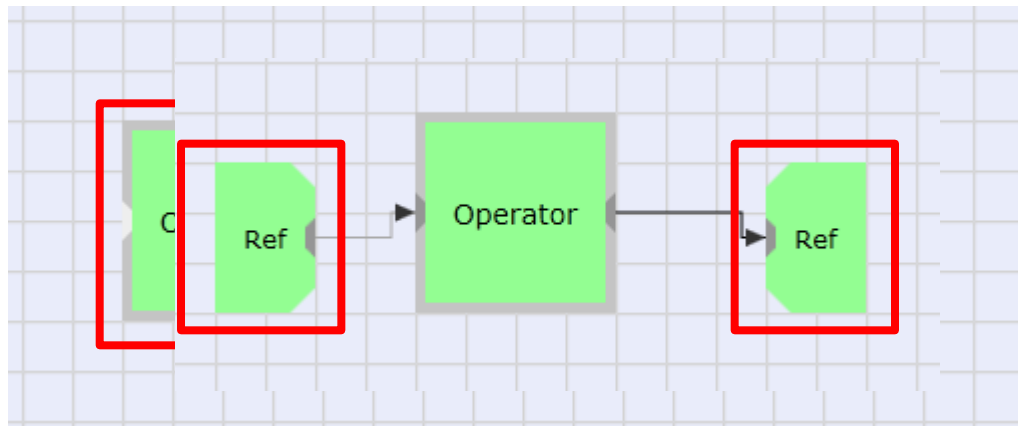


Program on visual programming language VPL

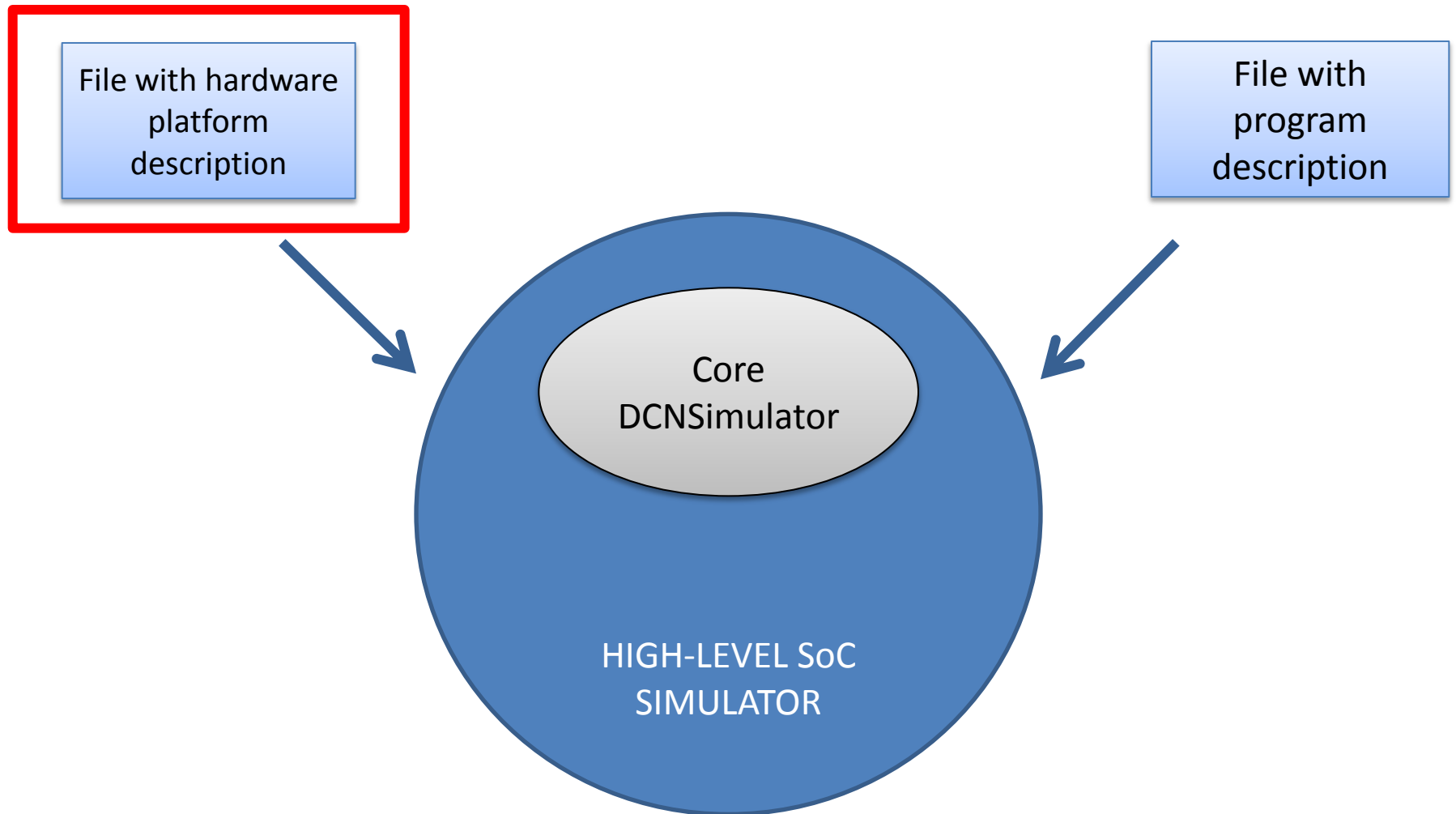


VPL Language objects types

- Operators
- Data
- Links
- Structures (subprograms)
- References

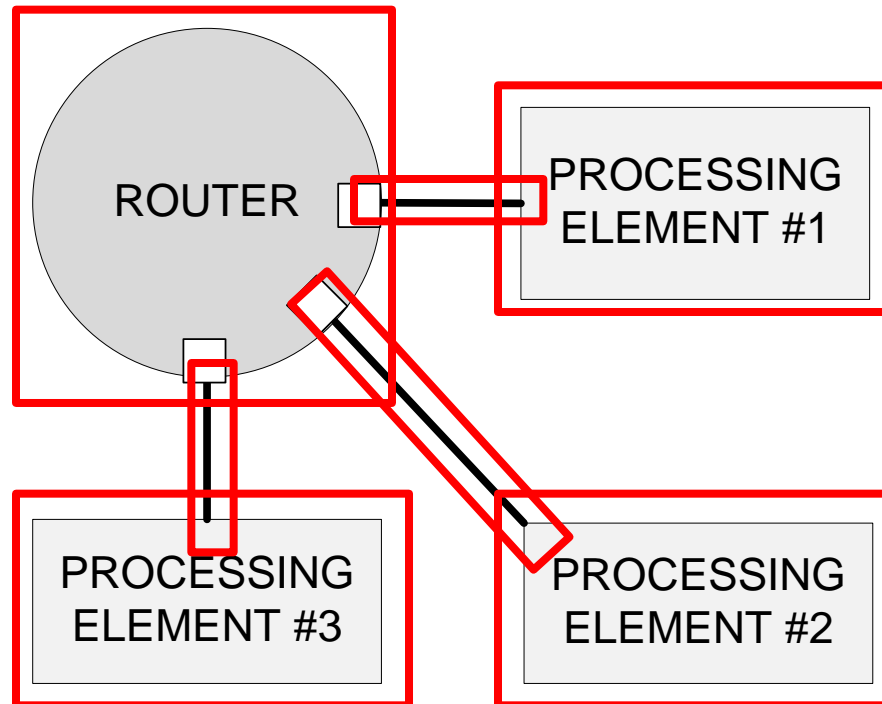


Simulator's structure



Hardware configuration

- Channels
- Processing elements
- Routers

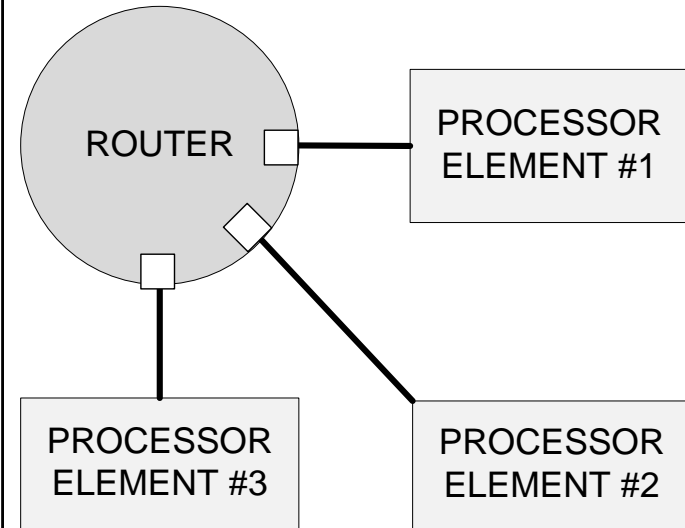


Hardware configuration

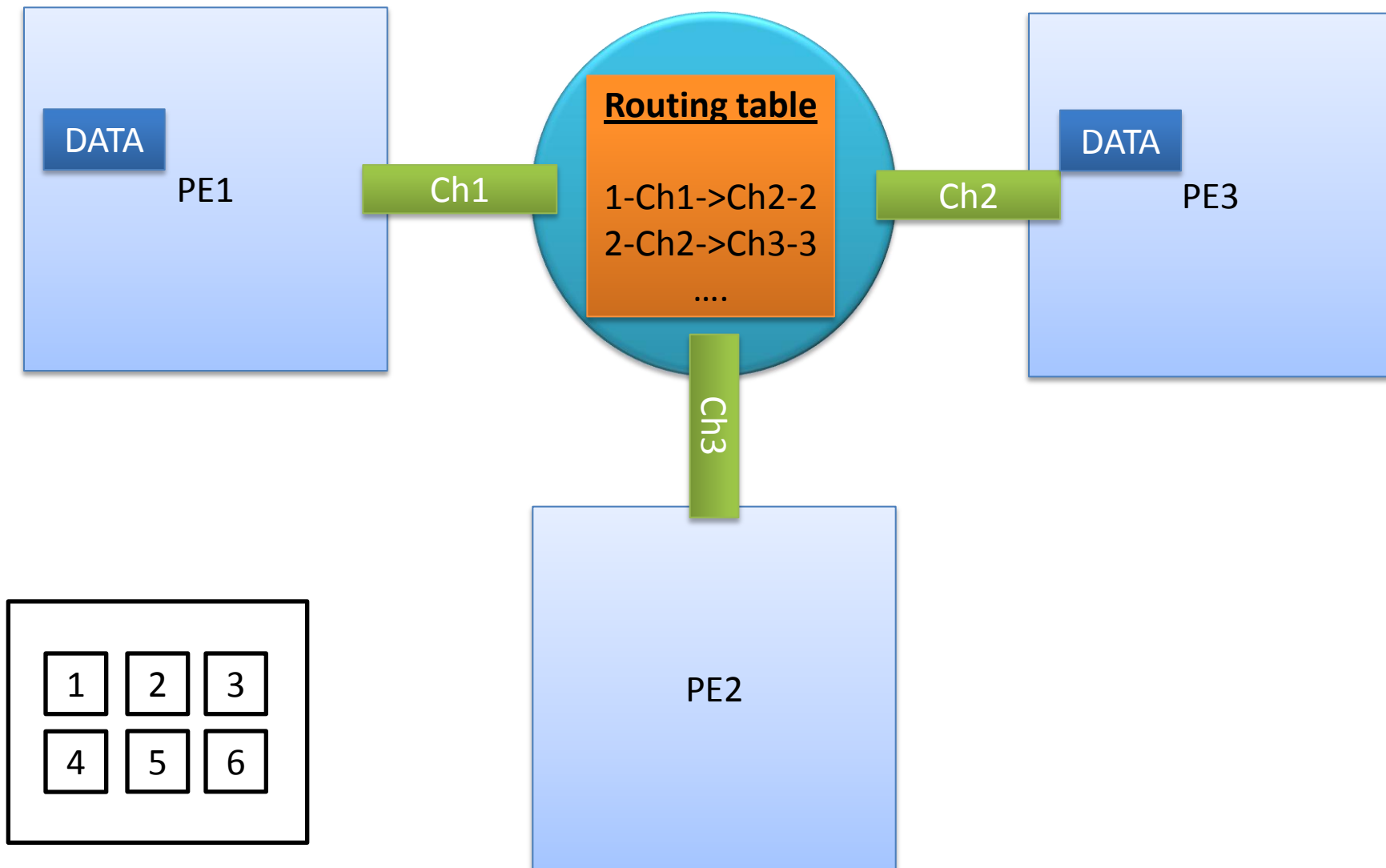
Configuration file

```
<?xml version="1.0" encoding="UTF-8"?>
<platform>
  <devices>
    <pe name="PE1"></pe>
    <pe name="PE2"></pe>
    <pe name="PE3"></pe>
    <router name="Router1"></router>
  </devices>
  <channels>
    <channel src="Router1" dst="PE1" ></channel>
    <channel src="Router1" dst="PE2"></channel>
    <channel src="Router1" dst="PE3"></channel>
    <channel src="PE1" dst="Router1" ></channel>
    <channel src="PE2" dst="Router1" ></channel>
    <channel src="PE3" dst="Router1"></channel>
  </channels>
</platform>
```

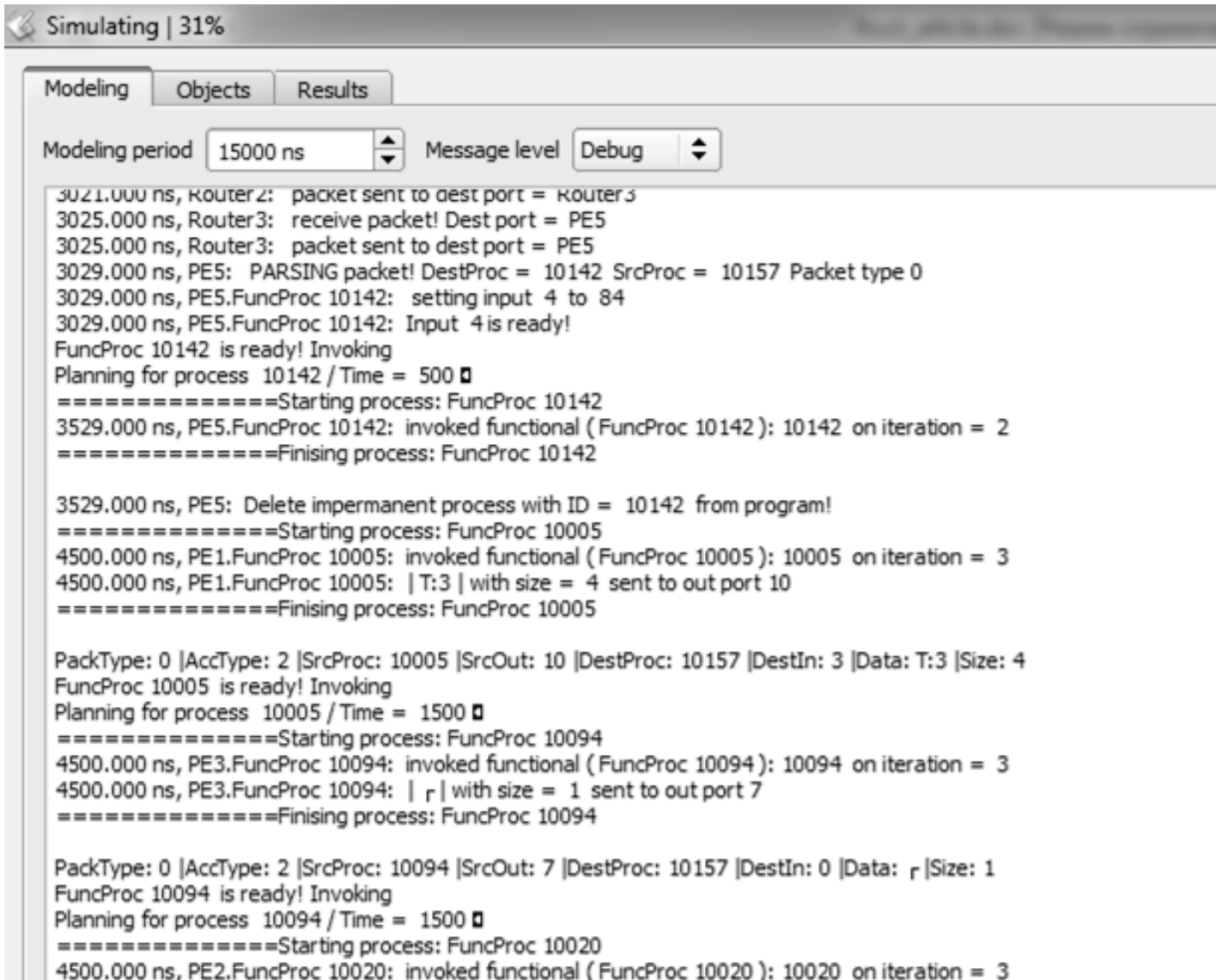
Hardware platform, which is described in file



Hardware platform preparation for Hardware platform description file parsing simulation



Simulator's window



Simulating | 31%

Modeling Objects Results

Modeling period 15000 ns Message level Debug

```
3021.000 ns, Router2: packet sent to dest port = Router3
3025.000 ns, Router3: receive packet! Dest port = PE5
3025.000 ns, Router3: packet sent to dest port = PE5
3029.000 ns, PE5: PARSING packet! DestProc = 10142 SrcProc = 10157 Packet type 0
3029.000 ns, PE5.FuncProc 10142: setting input 4 to 84
3029.000 ns, PE5.FuncProc 10142: Input 4 is ready!
FuncProc 10142 is ready! Invoking
Planning for process 10142 / Time = 500
=====Starting process: FuncProc 10142
3529.000 ns, PE5.FuncProc 10142: invoked functional (FuncProc 10142): 10142 on iteration = 2
=====Finising process: FuncProc 10142

3529.000 ns, PE5: Delete impermanent process with ID = 10142 from program!
=====Starting process: FuncProc 10005
4500.000 ns, PE1.FuncProc 10005: invoked functional (FuncProc 10005): 10005 on iteration = 3
4500.000 ns, PE1.FuncProc 10005: | T:3 | with size = 4 sent to out port 10
=====Finising process: FuncProc 10005

PackType: 0 |AccType: 2 |SrcProc: 10005 |SrcOut: 10 |DestProc: 10157 |DestIn: 3 |Data: T:3 |Size: 4
FuncProc 10005 is ready! Invoking
Planning for process 10005 / Time = 1500
=====Starting process: FuncProc 10094
4500.000 ns, PE3.FuncProc 10094: invoked functional (FuncProc 10094): 10094 on iteration = 3
4500.000 ns, PE3.FuncProc 10094: | r | with size = 1 sent to out port 7
=====Finising process: FuncProc 10094

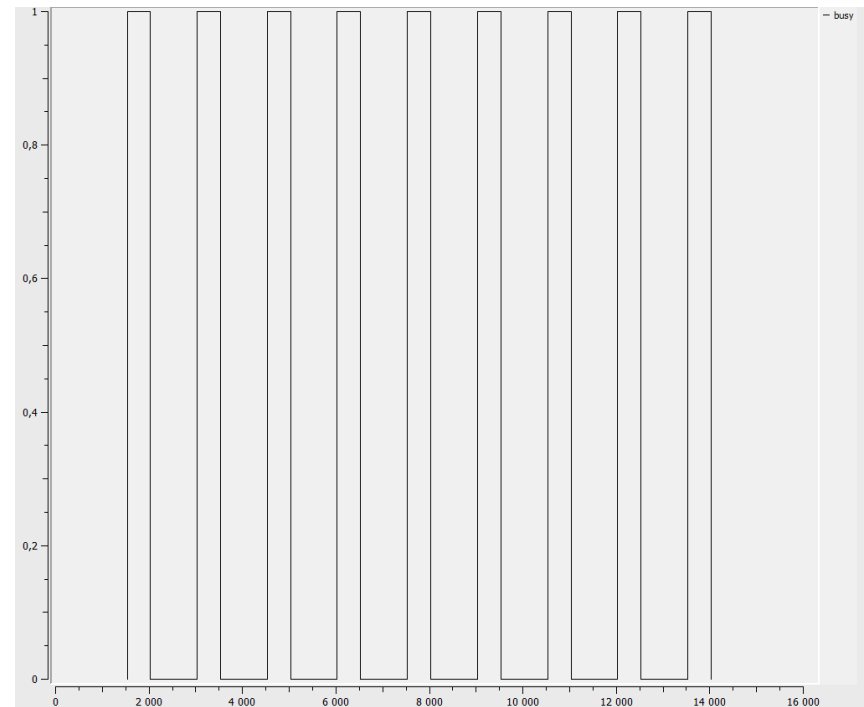
PackType: 0 |AccType: 2 |SrcProc: 10094 |SrcOut: 7 |DestProc: 10157 |DestIn: 0 |Data: r |Size: 1
FuncProc 10094 is ready! Invoking
Planning for process 10094 / Time = 1500
=====Starting process: FuncProc 10020
4500.000 ns, PE2.FuncProc 10020: invoked functional (FuncProc 10020): 10020 on iteration = 3
```

Statistic

**Text file with common statistic
about processes**

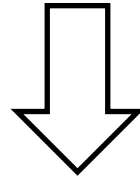
```
1500 ns: FuncProc 10005 is invoking on PE1 on iteration 1
1500 ns: FuncProc 10094 is invoking on PE3 on iteration 1
1500 ns: FuncProc 10020 is invoking on PE2 on iteration 1
1521 ns: IfProc 10157 is invoking on PE4 on iteration 1
2033 ns: FuncProc 10142 is invoking on PE5 on iteration 1
3000 ns: FuncProc 10020 is invoking on PE2 on iteration 2
3000 ns: FuncProc 10094 is invoking on PE3 on iteration 2
3000 ns: FuncProc 10005 is invoking on PE1 on iteration 2
3017 ns: IfProc 10157 is invoking on PE4 on iteration 2
```

**Processing element
occupation graphic**



CONCLUSIONS

- High-level simulator allows to model and debug high-level software representation for SoC model



It helps to solve the task of time reduction to market

**THANK YOU FOR
ATTENTION!**