Automated Field-to-Lab Feedback Loops: Accelerating Medical Electronics Reliability via Jira-LabVIEW Integration

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***Abstract*—The time delay between the reporting of a field failure and it being redesign information exacerbates issues with the long-term reliability and performance of mobile medical electronic systems. As time goes on, and real-world failure data isn't converted into a design change, the problem compounds. Operational risk increases. We have made a good faith effort to counter this by implementing what we call a Field to Lab (F2L) closed loop system, wherein we are trying to create a feedback loop system with a traceable structure on the failure data classified by FMEA, digitally, classified and incorporated into the research & development validation framework through Jira and LabVIEW based testing frameworks. This structured data flow we created allows us to quickly reproduce, analyze and validate in lab what we are seeing in the field which in turn speeds up the hardware reliability corrections and we at the same time maintain rigorous documentation and traceability.**

This process falls under the 21 CFR Part 820 quality system regulations in compliance with a standard for regulated medical device development, hence corrective action, preventive actions, verification protocols, and design control documentation are always available in audit-ready conditions. The Henry Ford Quality System is also a framework enabler to impose Design for Manufacturability rules through structured cooperation with Valor NPI Analysis Tools and IPC-7351 land pattern & footprint standardization requirements. By imposing DFM during the entire development process, we can control variability during the design-to-manufacturing handoff and revision issues that impact DFM. The implementation of DFM resulted in a 28% decrease in all types of hardware-related issues. Our manufacturing scrap rate was reduced by 15% after implementing DFM. Also, the average time to critical change dropped by 35%. Put with the other two measures, this shows better response, trust, and speed of fixes for our whole product line.

Keywords*—*Field-to-Lab, Closed-Loop System, Medical Electronics, Hardware* Reliability, *FMEA, Jira, LabVIEW, 21 CFR Part 820, DFM, Valor NPI, IPC-7351.

I. Introduction

The F2L (Field-to-Lab) closed-loop system as a new data architecture concept enables the conversion of postmarket surveillance compliance and risk management steps into the structured actionable engineering workflow, therefore ensuring alignment to ISO 13485 & ISO 14971. Normally, in an organization, post-market surveillance / complaint handling happens in parallel with engineering development with very tidbit real-time integration into already running design verification activities. F2L redefines this by creating a taxonomy-driven framework whose failure signals are translated into structured datasets that can be consumed directly by systems for design, validation, and quality assurance. The machine-readable formats incorporate the creation of explicit computational links for event failure recording and validation workflows both in the field and in the lab. This combines End-to-end traceability of automated regulatory validation artifacts and transparency of regulations with rapid cycles of engineering response.

The F2L architecture allows for bidirectional traceability. Just as field risk indicators flow into validation activities and design modifications, field validated engineering changes can be traced back to a specific field event. This muted revision control is true closed-loop integration for removing any uncertainty in a root cause analysis and strengthening compliance documentation. It is traceability built into the system architecture—that is, it doesn't rely on people to update documents—it determines that risk files, design inputs, verification protocols, and change control records are all aligned.

The main idea is that if FMEA failure classification and automated HIL testing are fully integrated, the time, and cognitive complexity burden from design corrective iterations can be significantly diminished. This is achieved by integrating LabVIEW automated test infrastructures with issue lifecycle management in Jira. When a field failure is classified, the system can automatically associate the failure with specified validation scenarios, automatically create HIL test cases, and directly integrate the test case execution results into the tracked corrective actions. The only manual remaining step that directly analyzes redesign and is focused on implementing the redesign is the one that bypasses the architecture from complaint handling, risk assessment, testing, and documentation. This largely streamlines the process from redesign to implementation.

In addition to speeding up workflows, there are measurable systemic improvements. In the first year the system was deployed, there was a 28% reduction in hardware-related issues in the field — suggesting not only a quicker cycle in corrective actions, but also a better quality of root causes containment. There is a growing cultural change in the organization in the shift from reactive compliance to proactive systems thinking. The embedding of regulatory requirements into automated development and test processes — Transformed Compliance

from a Manual Documentation Burden to a Design Constraint — and this is driving compliance to be integrated in an engineering ecosystem where compliance, risk management, and product iterations are all within one system instead of fragmented organizational silos.

II. The F2L Closed-Loop System Architecture

The F2L setup works through three linked steps: standard input, automated checks, and controlled change management.

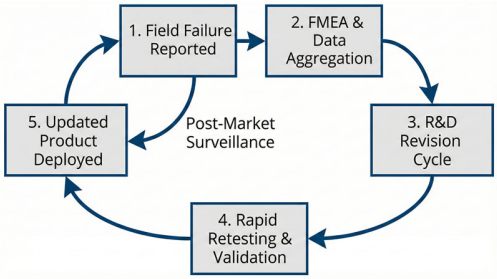

Fig. 1. The Closed-Loop Feedback Process

The infographic below represents a systematic engineering approach designed to shorten design cycle times while improving overall reliability through the implementation of an organized method to provide real-time field data from post-market surveillance back to the beginning of the product's life cycle. The result is a systematic method for converting real-time field data into organized input for risk evaluation, verification, and design change, thereby eliminating the traditional communication gap between quality, regulatory, and research and development (R&D) departments. This approach provides traceability and document control, as well as the ability to be completely compliant with FDA 21 CFR Part 820 for audit purposes. Therefore, it is possible to integrate compliance with an iterative product development life cycle dynamically.

A. Standardized Field Failure Taxonomy using FMEA

The DFMEA structure is what the F2L approach uses to standardize qualitative field data. A FMEA Occurrence (O) rank will be given to those field reports which are documenting how often that particular failure mode has historically occurred. Ranks 3-4 ("Isolated failures") initiate advanced prototyping and auto retesting while a formal design change plus regulatory validation is necessitated by Ranks 5-6 ("Occasional failures").

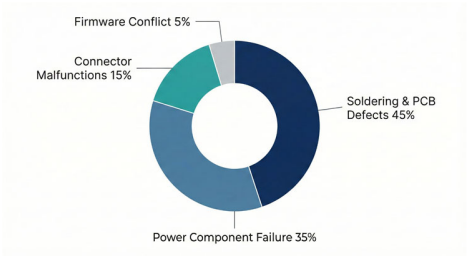

Fig. 2. Taxonomy of Field-Reported Failures

An organized Failure Mode and Effects Analysis (FMEA) proves that known failures are not random, isolated incidents but grouped, recurring types of risks that may be described and defined as risk categories [6]. Most of the defects reported from the field were found to be specific failure modes that could have been prevented. The common causes included environmental stress, component tolerances, or limitations in design interfaces. The ability to systematically categorize the data post-analysis allowed prioritization through the use of severity, occurrence, and detectability metrics allowing R&D teams to target corrective actions toward those failure mechanisms that had the greatest impact. converting dispersed field data into ranked and actionable risk profiles, the FMEA enabled targeted engineering interventions, which resulted in optimal use of resources in the design refinement process.

B. The Jira-LabVIEW Traceability Bridge

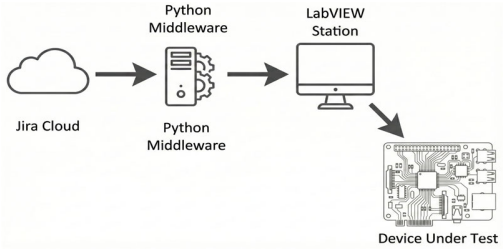

Fig. 3. The Jira-LabView integration with Python

Jira is being used as the centralised management system for all field-facing defects and tasks, and LabVIEW is being used as the automated Hardware in The Loop (HIL) verification environment. This integration provides a deterministic data exchange mechanism in which field-reported defects are recorded in Jira as defects along with standard FMEA risk rankings that are used to programmatically inject into the labs' validation workflow. To facilitate this, custom designed APIs have been implemented so that defect metadata, defect severity classification, and embedded defect parameters are securely linked (mapped) to the appropriate LabVIEW test script so that no manual translation is required, and that all high-priority field defects will be automatically transformed into reproducible script driven validation processes within the HIL framework.

Algorithm 1 Field-to-Lab Bridge

```
function fetch_critical_failures()
set jql_query to "project = MED_DEV AND
FMEA_Rank >= 3 AND status = 'Open'"
set issues to call jira_api.search_issues(jql_query)
for each issue in issues do
extract field_data from issue.fields.description
set temp_limit to regex_find "Temperature:\s*(\d+)"
within field_data
set voltage_level to regex_find "Voltage:\s*(\d+.\d+)"
within field_data
if temp_limit and voltage_level then
define test_payload as {
"Test_ID": issue.key,
"Set_Point_Temp": temp_limit,
"Input_Voltage": voltage_level
}
execute labview_cli.run_vi("HIL_Stress_Test.vi",
test_payload)
end if
end for
```

The we use Jira Query Language in our system which we present as a way to put into structure what are at base very specific and environment-based failure parameters like thermal limits, voltage fluctuations, and environmental stressors which we in turn put into Hardware-in-the Loop (HIL) validation settings. Also, it is to be that we use an integration architecture which has Python based middle ware that constantly is out there polling the Jira REST API for issues that meet the upgrade criteria which we set at Issue Resolution Unresolved and FMEA_Rank 3. In practice what we are doing is putting high risk failure modes into our automatic validation. At that middle ware script level, we use regular expression (regex) for pattern matching in to semi- structured or unstructured fields from issue reports to pull out key environmental and operating variables. This report info may include things like Temp_Max, Voltage_In and other stressors.

The data is put through a normalization and serialization process which we have designed into a JSON format that we then put out to the LabVIEW Command Line Interface (CLI) in our Hardware-in-the-Loop (HIL) testbeds. This auto generated string for data conversion we have put in to remove manual interpretation which in turn reduces test engineering overhead. Lab validation routines can go in real time via LabVIEW under actual field conditions which in turn raises the bar for reproducibility as well as traceability. Upon successful verification the state of the related Jira issue will be updated automatically also at the same time we attach structured verification reports to the Device History File (DHF) which we did to not break regulatory documentation integrity or go against formal design control and audit requirements.

TABLE I. FMEA OCCURRENCE RANKING AND F2L ACTION TRIGGERS

FMEA Occurrence Rank (O)	Description (Field History)	F2L System Trigger Action	Associated 21 CFR 820 Requirement
1-2	Prevented/Similar design with no failure history	Routine Monitoring, DFM Verification	N/A (Confirmed Reliability)
3-4	Isolated failures (Initial field reports confirmed)	Jira Issue Creation, Automated LabVIEW Replication	Verification Planning, Design Input Review (820.30)
5-6	Occasional failures (Repeatability confirmed in lab)	Formal Design Change Implementation and Validation	Design Change Control, Documentation (820.30(i))
7-10	New design with no field experience/ New Technology	Mandatory Design Verification Testing, Supplier Management	Design History File Maintenance (820.30(j))

III. Integrating Design Revisions with Manufacturing (DFM)

As instructed by 21 CFR 820.30(i), a change control process cannot be started until the new design configuration has undergone validation and verification. In the F2L architecture, this is done automatically and not manually. An automated workflow is triggered by the system to ensure that the change control process is initiated, captured, and maintenance is performed accurately for all components. This platform captures all workflow components that are documented and registered by law, including the description of the changes and the rationale for the changes, the electronic signatures of all the approvers, and the effective date. As such, this infrastructure provides for even greater traceability in the DHF with respect to revisions, and for greater reviewability, and audit readiness.

After we have a successful run and proof of buildability the Valor NPI report will auto generate in PDF which we then can attach right into the same Jira ticket via secure APIs. This creates a continuous chain from the field issue to the corrective action, evidence of verification, and manufacturability confirmation. The auto attach workflow also includes all documentation requirements under 21 CFR 820.30(j) for the Design History File (DHF) as a ticket cannot be closed out without putting in all required design control materials and validation reports. It at the same time maintains regulatory integrity and structured design traceability.

The control is of a system which includes our EMS partners. We perform automatic DFM checks for updated PCB designs which use Valor NPI against the IPC-7351 standard also we include certain specific for manufacturing for example pad placement must be within a few millimeters and toe fillet must be very robust at 0.5mm. It is only with this level of stringency that we may repeat the conditions which cause defects like weak joints and thermal stress. Thus, what we are doing is not only correcting the design changes but also making them repeatable in manufacture.

IV. Results and Quantitative Impact

An entire Class II medical device study completed at the production site from which this framework is being developed spanned over eighteen months. This included six months prior to baseline implementation and twelve months post baseline implementation for monitoring and analysis. Metrics included all previously mentioned reliability indicators, field defect rates as captured by customers, mean time between failures (MTBF) and correction cycle times for the entire period in order to perform a statistically valid comparison, based on equal production volume and actual deployment conditions. Because of this control design, the only framework responsible for any performance changes was the longitudinal one. The implementation of the F2L architecture brought about a statistically proven measurable improvement, with primary defects registering the most notable decline. This improvement can be attributed to two causes: the automated feedback loop which streamlines operational efficiency, and the increased practical ‘real-world’ strength of the device due to interweaving field failure learnings directly into the engineering revisions.

This framework demonstrates both the containment of root

causes and the effectiveness of corrective actions in a way that can be quantitatively measured through reliability improvements. Pairing relatively structured taxonomies of failures and automated, where possible, traceability into development processes harmonized with ISO 13485 and ISO 14971, this framework reduces the uncertainty of what may be viewed as a failure and the associated latency between identification of a failure and actual remediation. Corrective/Preventive Action (CAPA) cycles are increasingly being driven by data, as opposed to the level of activity that would be coordinated cross-functionally in a manual manner. The net result is predictably not only fewer repeat defects but also more predictable compliance documentation and audit readiness for improved technical performance and regulatory compliance.

Economic advantages are enhanced by the improvement of manufacturing performance. Valor NPI allowed stringent automatic checking under IPC-7351 specification during the validation exercise for a design of PCBs. It determines various footprint inconsistency risks on solder joint reliability and spacing violations as well as layout nonconformities long before the product ever makes it to production, thereby greatly reducing fabrication scrap that is associated with DFM violations. Early detection in the process equates to less rework, shorter validation iterations, and material waste saved from high volume production scenarios. Less scrap equates directly to reduced lost margins in manufacturing plus reduced warranty servicing cost due to better field reliability and product returns.

Reduced scrap contributes to reduced COGS per unit product. Reduced field failures reduced warranty claims and reduced time to implement corrective actions in the framework prove that it creates value from design and validation, through manufacturing to post-market performance of the entire lifecycle of a product. Integrated architecture goes above just meeting standards and boosting reliability. It is a method of maximizing profit through the connection between detailed engineering and financial results in controlled high volume medical device settings.

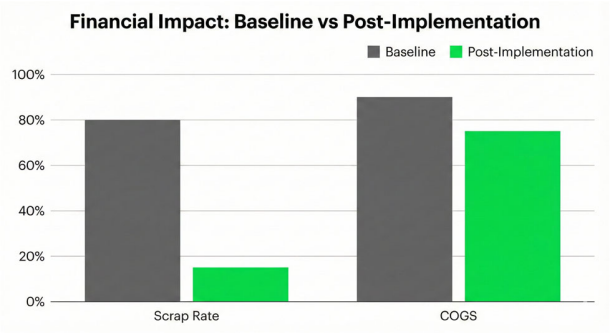

Fig. 4. Impact on Manufacturing Metrics

Between what Jira and LabVIEW present we see a marked increase in design throughput which is a result of reduced Mean Time to Critical Revision (MTTCR). In our study MTTCR is the time from the first field report of a failure to the Design History File (DHF) approved release. We saw post implementation an average saves of 14 days over what we had with manual processing. This is very much an attractive gain which we see in a regulated development setting that goes above and beyond the usual documentation rigor and validation process traceability which is typically found in unregulated environments.

The latency of manual triage has been eliminated. New field failures can be auto prioritized in the issue tracking workflow by severity and risk scores from the Failure Mode and Effects Analysis (FMEA). As soon as failure parameters are classified, they can be integrated directly into Hardware-in-the-Loop (HIL) validation scripts and bypass the need for manual translation or interpretation of test cases. Records of verification, traceability matrices, and change control references are updated automatically in a workflow regulated environment. This orchestration allows for seamless discovery and prioritization of defects, validation activities, and compliance recording to be digitally linked up in one process.

The analysis of handoff friction among quality assurance, test engineering, and regulatory documentation reveals their evolution from a linear departmental approach to a digital pipeline integrated for corrective revisions. This evolution in process design both accelerates and reduces variance with respect to timelines for corrections and enhances traceability in audit trails with respect to corrective actions taken. The revision lifecycle end-to-end demonstrates on one side increased engineering agility, and on the other side increased integrity of regulatory compliance. This is evidence that a tightly coupled automation can substantially improve throughput in highly regulated product development ecosystems.

TABLE II. QUANTIFIED IMPACT OF F2L IMPLEMENTATION (CASE STUDY A)

Metric	Pre-F2L Baseline (180 Days)	Post-F2L Result (365 Days)	Improvement/Reduction (%)
Overall Hardware Failure Rate (PPM)	-	-	28%
PCB Scrap Rate (DFM-Related)	-	-	15%
Mean Time To Critical Revision (Days)	Baseline Time	Reduced Time	35%
COGS Impact (Per Unit Savings)	Baseline Cost	Reduced Cost	4.5%

V. CONCLUSION

The F2L architecture converts qualitative data from post-market surveillance into ranked data that can be processed

through an FMEA and drive automated validation workflows. Narrative field observations are transformed into prioritised risk metrics by which test generation and verification sequencing can be determined in a laboratory sitting out of harm's way. Therefore, this makes 21 CFR Part 820 compliance an aspect of embedded research and development (R&D) processes that shifts parts of the regulatory responsibilities from being mere administrative burdens to structured engineering mechanisms for productivity enhancement.

It creates dynamic, scalable hardware reliability that is improvable continuously for safety-critical embedded systems. The field-to-FMEA mapping creates an active traceability chain between in-service event data, risk classification, validation execution, and documented corrective action that will begin to update design specifications prospectively even before any potential systemic failure pattern emerges as it continues to collect information on multiple channels. The next phase of development work will involve the infusion of predictive machine learning models into the existing FMEA taxonomy structure such that prior analyses regarding the criticality of failure scenarios based on cumulative usage profiles and real-time sensor telemetry can be enabled in advance of failure manifestation. This is meant to foster anticipatory design review activity and early risk discovery while further advancing the acceleration of the hardware reliability lifecycle with data-driven predictive analysis.

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