Using P-median Algorithm for 3D Network-on-Chip Design

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***Abstract*—In the paper we describe P-medians searching algorithm for Three-dimensional (3D) Network-on-Chip (NoC) design. Modern 3D NoC development is complex and complicated task. Developer should solve different problems: IP blocks placement on the die, organization of vertical links between dies in the 3D stack, energy consumption limitation, system performance improvement. We consider approaches for placement vertical links on the die and suggest a new algorithm that is based on the P-median problem.**

I. Introduction

Developing of modern communication system inside chip aid the appearance of Three-dimensional (3D) Network-on-Chip (NoC). It is new trend in field of communication subsystem on an integrated circuit design. 3D NoC is an emerging technology that has the potential to achieve high performance with low power, [1].

The number of IP blocks that make up the chip grows. This is associated with the development of chip manufacturing technologies. The process technology is decreased and there are already devices on the market which are made on 14 nm process technology. For example, Samsung provide Exynos processor from Octa 7 family according to this technology [2]. Intel Core M processors are based on 14 nm process technology. Through three-dimensional tri-gate transistors 2nd generation 14-nanometer technology provides industry-leading performance, energy efficiency, density and value of each transistor and is used to produce a wide range of products: from high-performance computers to systems with low power consumption.

According to the International Technology Roadmap for Semiconductors (ITRS), the number of transistors integrated on a chip continues to grow [3]. Traditional 2D integration can hardly handle such a design complexity in the future. It will result long global wire lengths, causing a high delay, high power consumption and low performance [1]. These parameters are very critical for new advanced systems. Hence, to continue the progress of Moore's law, 3D integration is introduced by stacking multiple dies vertically. The 3D integration becomes a promising alternative because it can potentially offer higher device density, providing shorter wire lengths and faster on-chip communication compared with the 2D integration.

A 3D chip contains multiple dies vertically stacked together. There are different approaches for interconnection dies with each other. They are Through-Silicon-Via (TSV), die-to-wafer, flip chip.

We focus on TSV. TSV is a viable solution in building 3D chips by stacking IC layers together using vertical interconnects. These interconnects are formed through the silicon die to enable communication among layers.

II. The complexity of 3D system design

The TSV technology provides new opportunities for increasing the number of vertical interconnection links between layers of chip also it helps to decrease wire length and therefore energy consumption of chip in general. Researchers claim that the key thing for good 3D system development is placement of TSVs. The number and location of TSVs influence quality and robustness of 3D system, [4].

Therefore it is necessary to put interconnection points on chip effectively according to certain rules. Possible solution to this problem can be selected from two options: regular or irregular placement of TSVs, [5]. It is clear that operation characteristics of the whole 3D system depend on data exchange patterns of IP blocks located on different layers. For example, if processors are located on one layer and memories are located on another then we should use several TSVs to not have bottleneck in the system.

Also it makes sense to note that TSVs also occupy a certain area on the chip. The TSVs area depends on the process technology of chip. When we use 45 nm process each TSVs occupies 2.47 um × 2.47 um. If TSVs number optimization is not taken into account then total area of all layers of 3D system can get bigger than corresponded area of 2D system.

When moving from 2D technology to 3D technology, some components may require changes in order to use features of 3D technology.

The widely used topology of 2D system is mesh. The structure of switch consists of 5 ports, switch fabric and buffers, (Fig.1). When moving from 2D technology to 3D technology, the number of ports are 7. One port is used for data transmission to upper layer. One port is used for interconnection to down layer. Increasing of ports leads to complication of switch fabric and arbitration block, [6]. In article [7] the authors provide information about area and energy consumption of switch fabric 5x5. The area is 8523 μm2 and energy consumption is 4.21 mW. When the number of ports equal 7, then the area is 17289 μm2 and energy consumption is 9.41 mW. The process technology is 90 nm, the frequency is 500 MHz. It turns out that the area increases 2 times, and energy consumption - 2.2 times. Therefore if each switch of 3D system has 7 ports then the total system area and energy consumption would be very high. It is additional parameter which affects on the number of TSVs.

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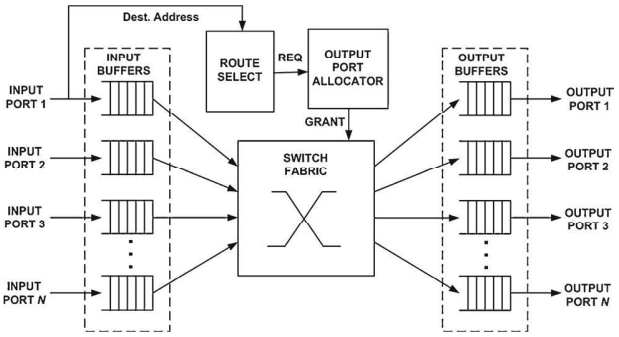

Fig. 1. Architeture of switch

The authors of article [8] present methods for allocating and placing a minimal number of vertical links and the corresponding vertical routers to achieve specified performance goals. According to their method a good placement should satisfy the following requirements: 1) each node shall reach at least one TSV within a specified distance; 2) the number of TSV in topology shall be as small as possible; 3) the TSVs shall be distributed uniformly over the topology. Fig. 2(a) shows a worst case placement of TSV in mesh network. In this configuration, the TSV is placed on one side of the chip, causing high delays on the other side of the chip. Fig. 2(b) shows an improved placement. In this configuration, node requires just one hop to access a TSV, which results in a minimal average hop count.

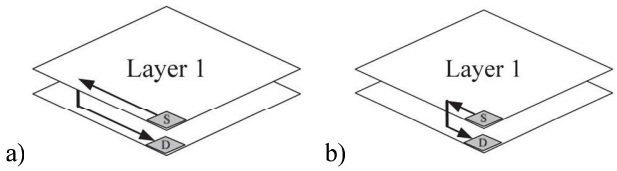

Fig. 2. Comparison TSV placement

The issue of finding an optimal placement of pillars in a network topology can be expressed as an optimization problem. Authors present an Integer Linear Programming (ILP) method that considers the above requirements to find an optimal placement. As shown in the some chars of article, the time required to find an optimal distribution grows fast with increasing topology size. In order to obtain placements for sizes larger than 17x17, researchers explore a Divide and Conquer strategy whereas placements of smaller topologies are used to create placements for large topologies. The main idea is division a large network into several smaller networks and using ILP method for them. The important disadvantage of this approach is non-minimal placement for network after concatenation small network in one big network, [8].

In the book [6] authors describe task of generation of the 3D stack and determination of the communication (routing paths) among layers. Fig. 3 (b,c) shows two alternative partition to layer assignments regarding the application's hypergraph depicted in Fig. 3 (a). The vertical lines in this figure correspond to TSVs. As we can conclude, the assignment depicted in Fig. 3 (b) needs 80 TSVs (45 TSVs between Layer1 and Layer2 and 35 TSVs between Layer2 and Layer3). On the other hand, the solution depicted in Fig. 3 (c) requires only 55 TSVs (20 TSVs between Layer1 and Layer2 and 35 TSVs between Layer2 and Layer3), without affecting either the functionality of target application, or its performance.

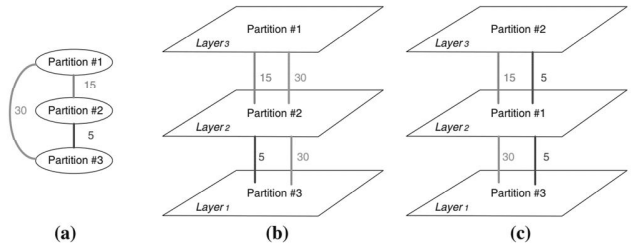

Fig. 3. Two alternative solutions derived (b and c) from partitioning to layer assignment for the same application (depicted in (a))

In the section 3 we consider our method for placement TSVs on chip which based on P-medians search algorithm.

III. Applying P-median for TSVs placement on chip

For each specific 3D system designer may independently calculate the required amount of TSV for communication on chip. Designer can use various approaches proposed by scientists from different countries. For example, if you know the area of the 2D chip, it is possible to calculate the maximum number of TSV, which can be used to build 3D (1), where total 3D area will not larger than that 2D area to a certain value (equation 1). Where N_{TSVmax} - the maximum number of TSV, S_{2D} - chip area according to the technology 2D, S_{3D} - estimated area of 3D chip, S_{TSV} - TSV area in according to the process technology.

$$N_{TSVmax} = \lfloor (S_{3D} - S_{2D})/S_{TSV} \rfloor \quad (1)$$

The area of the 2D chip in the same design technology will be less than the total area of the 3D chip, because the organization of vertical interconnections between layers requires more area under the TSV. But the wire length between the components of 2D system is longer than in 3D system.

As mentioned above, in addition to determining the number of interconnections between the layers of 3D system, there is an actual problem of their allocations within the chip. In this paper, we propose the method for searching TSVs placement inside the chip.

It is assumed that the designer defines the number of interconnections which must be placed in a single layer 3D chip. The proposed approach is based on the algorithm P-medians search in the graph, [9]. This algorithm has been modified for use in the design of 3D systems.

The basic idea of the algorithm P-medians search in the graph is reduced to the definition of the graph vertices that are on the minimum distance from the rest of the vertices. TSV location searching is necessary to find such placement, where the length of communication lines between the chip blocks and TSV will be as small as possible. In addition to the bond lengths in the design of 3D systems, there must take into account the data transmission characteristics between the blocks, disposed on different layers. Therefore it is necessary to consider the loading of the connections between the layers. Their load must be distributed as evenly as possible. Additionally, you must take into account the factor that the

TSV location must be sufficiently distant from each other, so as not to interfere with the transmission of signals.

The mesh is the most common topology of chip. The network topology is represented as a graph. We assume that nodes of the graph are switches and edges of the graph are links between switches. IP block of system are connected to switch.

TSV placement is performed taking into account the topology of the network switches interactions within a single layer.

The input data are:

- Submission of the topology switches interaction of the one layer 3D assembly in the form of a graph interconnections;
- The number of vertical links (TSV) between adjacent layers, referred to as P;
- The minimum distance, that must be between adjacent points location TSV, referred to as H;
- The deviation of the load TSV, referred to as d.

The main objective of the algorithm to find such nodes in the graph that will match the given constraints of the input data. From all possible solutions will be found a solution that will be characterized by the smallest distance between found nodes and other nodes of the graph. The found nodes will be the TSV location.

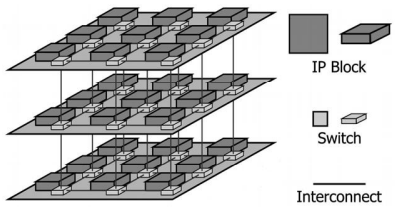

Fig. 4. Structure of 3D system

The algorithm to find the location of nodes consists of several steps:

Step 1. Find the shortest distance between all nodes of the graph using the wave algorithm.

Step 2. Construct a matrix in which the row corresponds to a node of the graph, and the column provides information about the node and its distance from the node corresponding to the considered row. The values of the columns are sorted in ascending order of distance. (The format is shown in the table)

Step 3. Find all the possible combinations of P nodes that are from each other by a distance greater than or equal to a given input parameter H.

Step 4. Choose from the list of solutions, that found in step 3, the solution, which will be satisfy evenly connection of nodes to the P-medians with the smallest distance to them.

A. *Construction of a distance matrix between nodes of the graph*

When constructing a distance matrix between nodes of the graph used wave algorithm for solving the same problem of searching the shortest route between the nodes of the graph, you can use the Ford-Fulkerson algorithm or other similar algorithms used to find the shortest paths in graphs.

Initially, between all pairs of nodes are determined the shortest distances (Fig. 6). Then, from the obtained data is generated the matrix according to the following structure (Fig. 7). The first column contains a list of all nodes in the remaining columns contain information which indicates how far from the node of the first column to the other nodes of the graph in ascending order. It should be noted that the distance between the nodes is considered to be in the number of ribs, which are between a given pair of nodes.

Node id / Node Id	1	2	3
1	0	1	2
2	1	0	1
3	2	1	0

⇦ The shortest distance between all nodes in graph

Fig. 5. The shortest distance matrix

Nodes id	Distance (node id)	
1	1(2)	2(3)
2	1(1)	1(3)
3	1(2)	2(1)

⇦ The sorted distance matrix in ascending

Fig. 6. The shortest distance matrix in ascending

B. *The calculation of the distance between the medians of the graph*

The vertical interconnections between layers of 3D assembly should not be placed closely to each other. This is necessary in view of the large heat release vertical links. Therefore it is necessary to place them at some distance from each other. In this approach, it is assumed that this distance is specified by the designer in the input data (parameter H).

It should be noted that the distance between the TSV locations is calculated according to the rule for calculating the distance Chebyshev. Chebyshev distance (L) is the maximum of modulus of the difference components of two vectors, the formula 2.

$$L(\vec{x},\vec{y}) = \max_{i=1,\dots,n}|x_i - y_i| \qquad (2)$$

Since we are working with the Mesh topology is convenient to represent nodes in the network as elements of a two-dimensional array. Each node has an index indicating the row [x] and column [y], in which the node is located. As the index value of x and y coordinates can be correlated with the switch position next to which will be located vertical line connections between the layers.

The condition for verifying the constraint on the distance between the medians is displayed in the following formula:

$$(|x_k - x_s| \geq H) \text{or} (|y_k - y_s| \geq H), \qquad (3)$$

Where x_k, x_s - index indicating a row of k-th and s-th node respectively; y_k, y_s - index indicating a column of k-th and s-th node respectively. If the condition is satisfied, then the k-th and the s-th nodes can be medians.

Thus, for each pair of median nodes is checked the restriction on the distance between them. For example, for the node with coordinates (3;3) and the limitation of distance H=2 to any other median node, you can select all the nodes that satisfy this constraint. Fig. 6 selected nodes that satisfy the constraint H=2 for a node with coordinates (3;3).

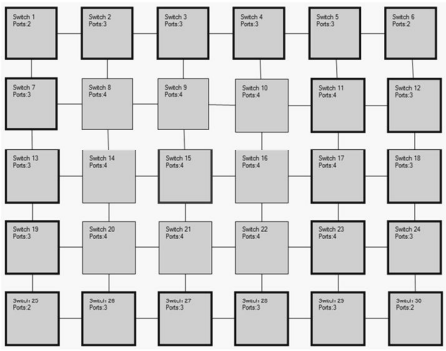

Fig. 7. Nodes that satisfy the constraint Dp=2 for a node with coordinates (3;3).

The following figures show examples not satisfying the constraint H=2 in the case of the three medians.

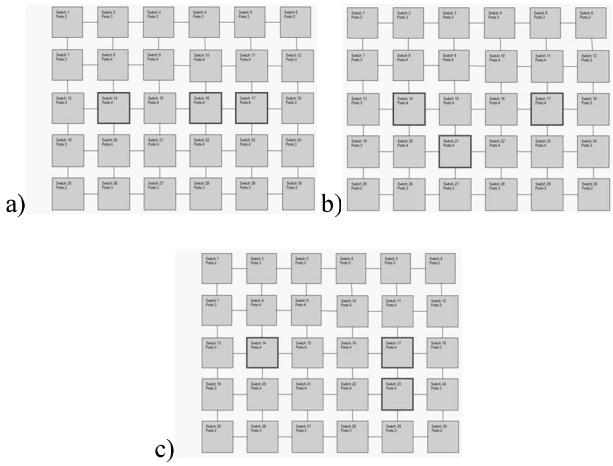

Fig. 8. Examples not satisfying the condition H=2 in the case of the three medians. a) fails the condition by columns; b) fails the condition by columns and by rows; c) fails the condition by the rows.

C. *Evenly distribution of serviced nodes between the medians*

Evenly distribution of serviced nodes between the medians is necessary for evenly loading of the vertical links.

The parameter d specifies the maximum allowable deviation from the average number of serviced nodes. This limitation can be expressed by the following inequality:

$$\frac{NN-P}{P} - d \leq NAN \leq \frac{NN-P}{P} + d,$$

Where NN - number of nodes in layer; P – the number of medians (nodes with TSV), NAN – the number attachable nodes each median.

For example, the network size 6x5 contains 30 nodes. You must place 3 TSV, the parameter d=1. The number of attachable nodes to each median must be in the range 8≤NAN≤10.

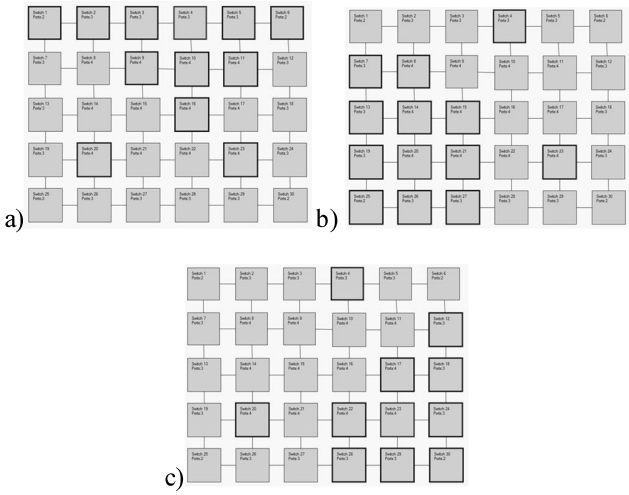

Fig. 9. Solution example for P=3, d=1. a) NAN_1=9; b) NAN_2=10; c) NAN_3=8

D. *An example of work of the algorithm*

Consider the example of the algorithm on a graph, which is derived from the 3x3 Mesh topology.

Consider the following example (Fig. 10)

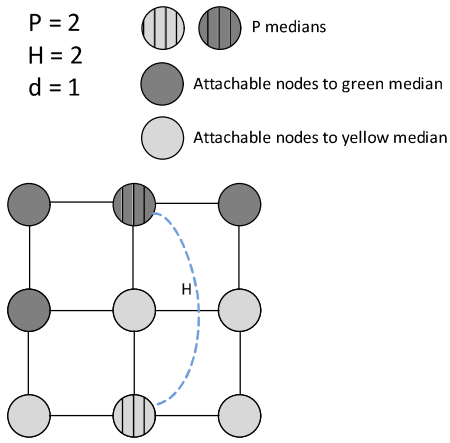

Fig. 10. The example of a graph with found P-medians

For this graph you need to find the 2 nodes that can be placed between each other no closer than at a Chebyshev distance of 2 hops.

Total in graph is 9 nodes, 2 of them will be selected as the P-median, the remaining 7 must be attached to each median, so that the distance between median and the attachable node is minimal possible. Unmedian nodes must as evenly as possible attached to the median nodes and their attachment does not go beyond the limits indicated in the input parameter d. It turns out that attachment in our case is 3.5 nodes to each median. It is impossible, since the nodes are indivisible. Hence three nodes will be attached to a first median, and four nodes will be attached to the second median. The shortest distance between

medians and attached nodes is 2. To find solutions with a smaller shortest distance is impossible for this input data.

As a result of the algorithm will be found the graph nodes that have the smallest maximum distance to other nodes and at the same time themselves be positioned with respect to each other by a distance not less than the designated input value; with the remaining nodes of the graph which are will evenly attach to medians.

IV. CONCLUSION

In this paper was considered the problem of placement TSVs inside 3D system. We proposed a search method for placement TSV based on the search algorithm P-median in the graph. The proposed method makes it possible to find a location of a predetermined number of vertical links at which achieves the minimum length of the wire between the blocks are located on a single chip and TSV, taking into account that distance between each TSV must be not less than specified value of parameter H, and all nodes in the layer should be evenly distributed within the parameters d, which is also determined by designer at the design stage 3D system.

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